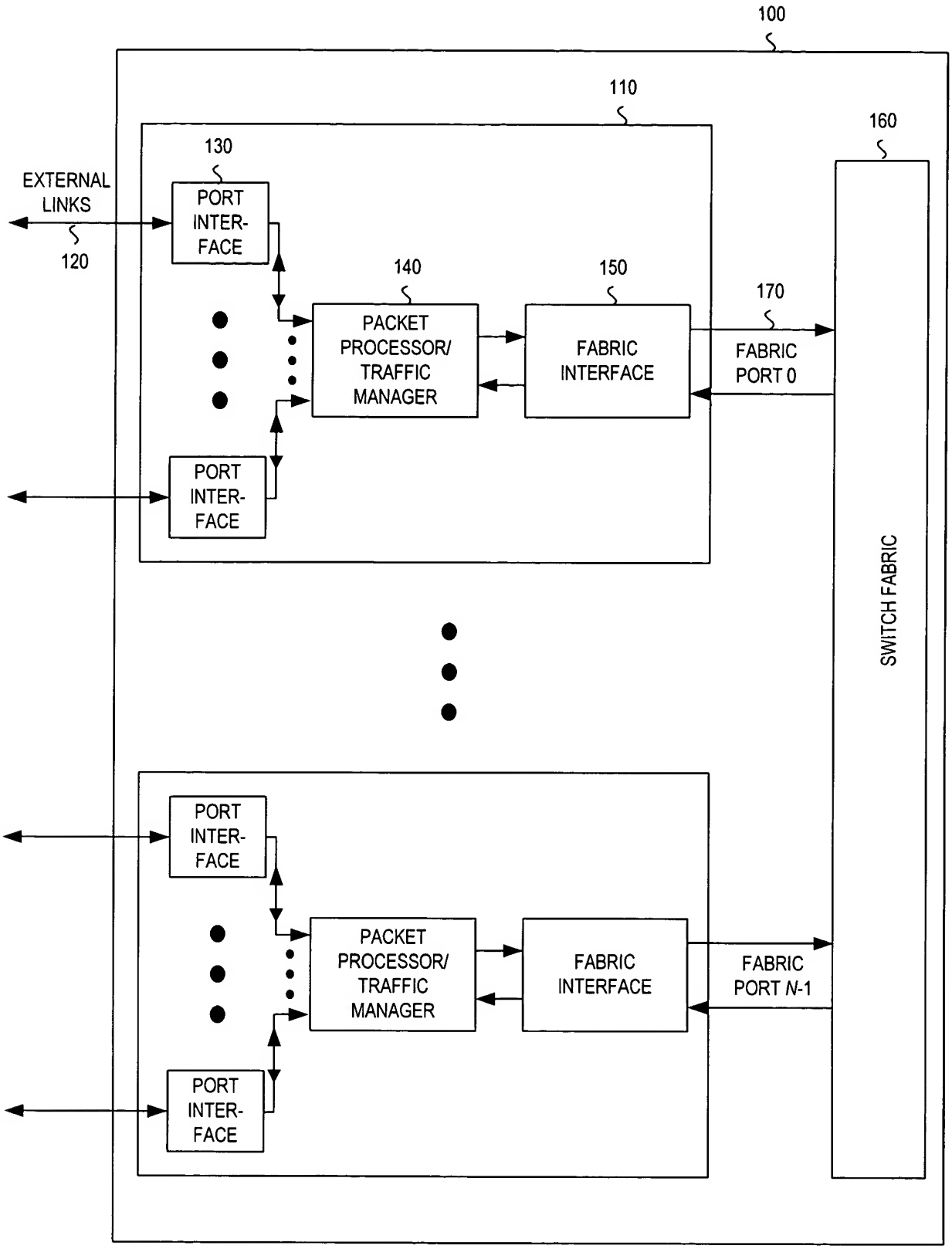

100
110
160
130
EXTERNAL LINKS
120
PORT INTER-FACE
140
150
170
PACKET PROCESSOR/ TRAFFIC MANAGER
FABRIC INTERFACE
FABRIC PORT 0
PORT INTER-FACE
SWITCH FABRIC
PORT INTER-FACE
PACKET PROCESSOR/ TRAFFIC MANAGER
FABRIC INTERFACE
FABRIC PORT N-1
PORT INTER-FACE

FIG. 1

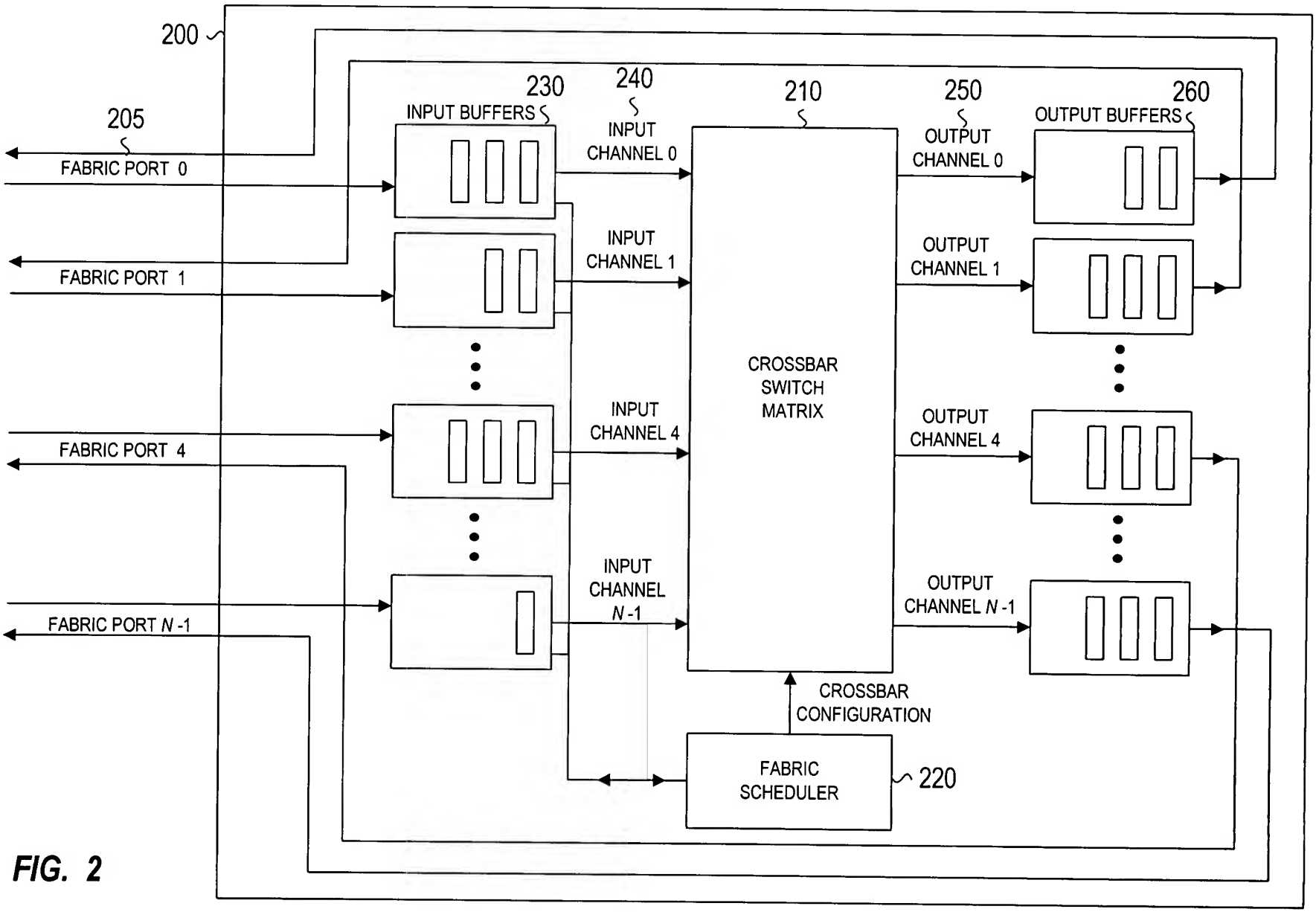

200
205
FABRIC PORT 0
FABRIC PORT 1
FABRIC PORT 4
FABRIC PORT N -1
230
INPUT BUFFERS
240
INPUT CHANNEL 0
INPUT CHANNEL 1
INPUT CHANNEL 4
INPUT CHANNEL N -1
210
CROSSBAR SWITCH MATRIX
250
OUTPUT CHANNEL 0
OUTPUT CHANNEL 1
OUTPUT CHANNEL 4
OUTPUT CHANNEL N -1
260
OUTPUT BUFFERS
CROSSBAR CONFIGURATION
FABRIC SCHEDULER
220

FIG. 2

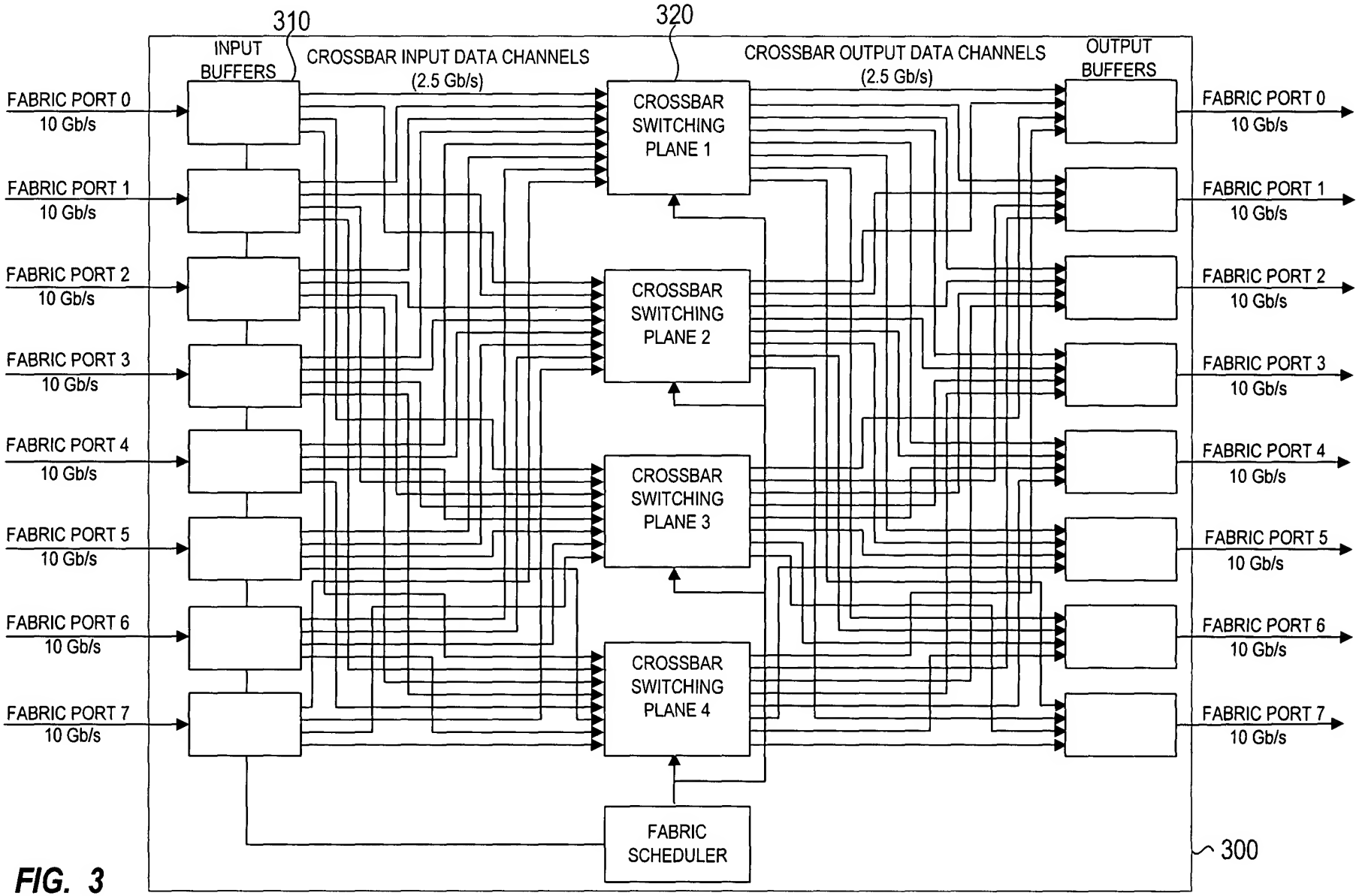

310
320
INPUT BUFFERS
CROSSBAR INPUT DATA CHANNELS (2.5 Gb/s)
CROSSBAR OUTPUT DATA CHANNELS (2.5 Gb/s)
OUTPUT BUFFERS
FABRIC PORT 0 10 Gb/s
FABRIC PORT 1 10 Gb/s
FABRIC PORT 2 10 Gb/s
FABRIC PORT 3 10 Gb/s
FABRIC PORT 4 10 Gb/s
FABRIC PORT 5 10 Gb/s
FABRIC PORT 6 10 Gb/s
FABRIC PORT 7 10 Gb/s
CROSSBAR SWITCHING PLANE 1
CROSSBAR SWITCHING PLANE 2
CROSSBAR SWITCHING PLANE 3
CROSSBAR SWITCHING PLANE 4
FABRIC SCHEDULER
FABRIC PORT 0 10 Gb/s
FABRIC PORT 1 10 Gb/s
FABRIC PORT 2 10 Gb/s
FABRIC PORT 3 10 Gb/s
FABRIC PORT 4 10 Gb/s
FABRIC PORT 5 10 Gb/s
FABRIC PORT 6 10 Gb/s
FABRIC PORT 7 10 Gb/s
300

FIG. 3

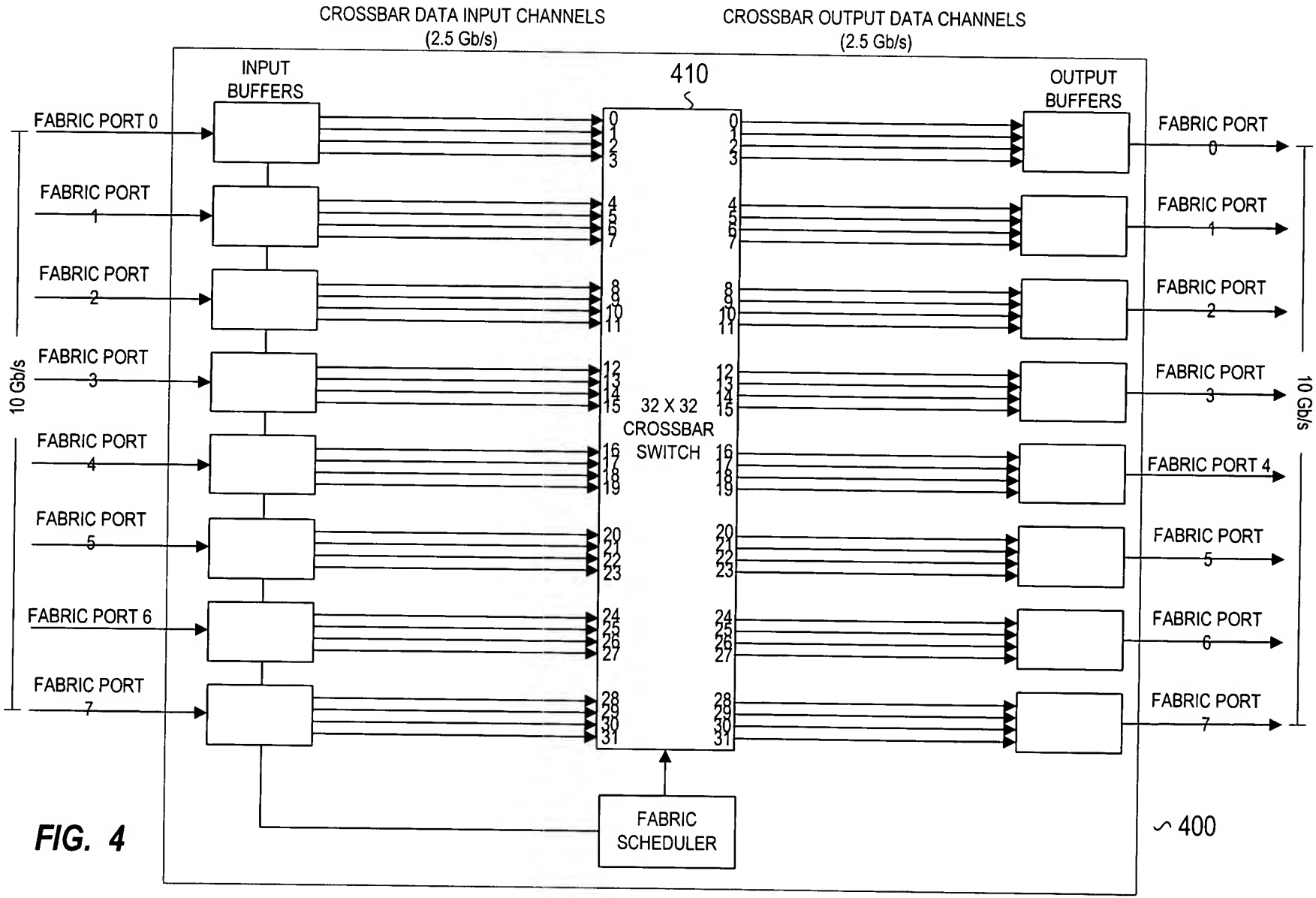

CROSSBAR DATA INPUT CHANNELS
(2.5 Gb/s)
CROSSBAR OUTPUT DATA CHANNELS
(2.5 Gb/s)
INPUT BUFFERS
410
OUTPUT BUFFERS
FABRIC PORT 0
FABRIC PORT 1
FABRIC PORT 2
FABRIC PORT 3
FABRIC PORT 4
FABRIC PORT 5
FABRIC PORT 6
FABRIC PORT 7
10 Gb/s
32 X 32 CROSSBAR SWITCH
FABRIC SCHEDULER
400

FIG. 4

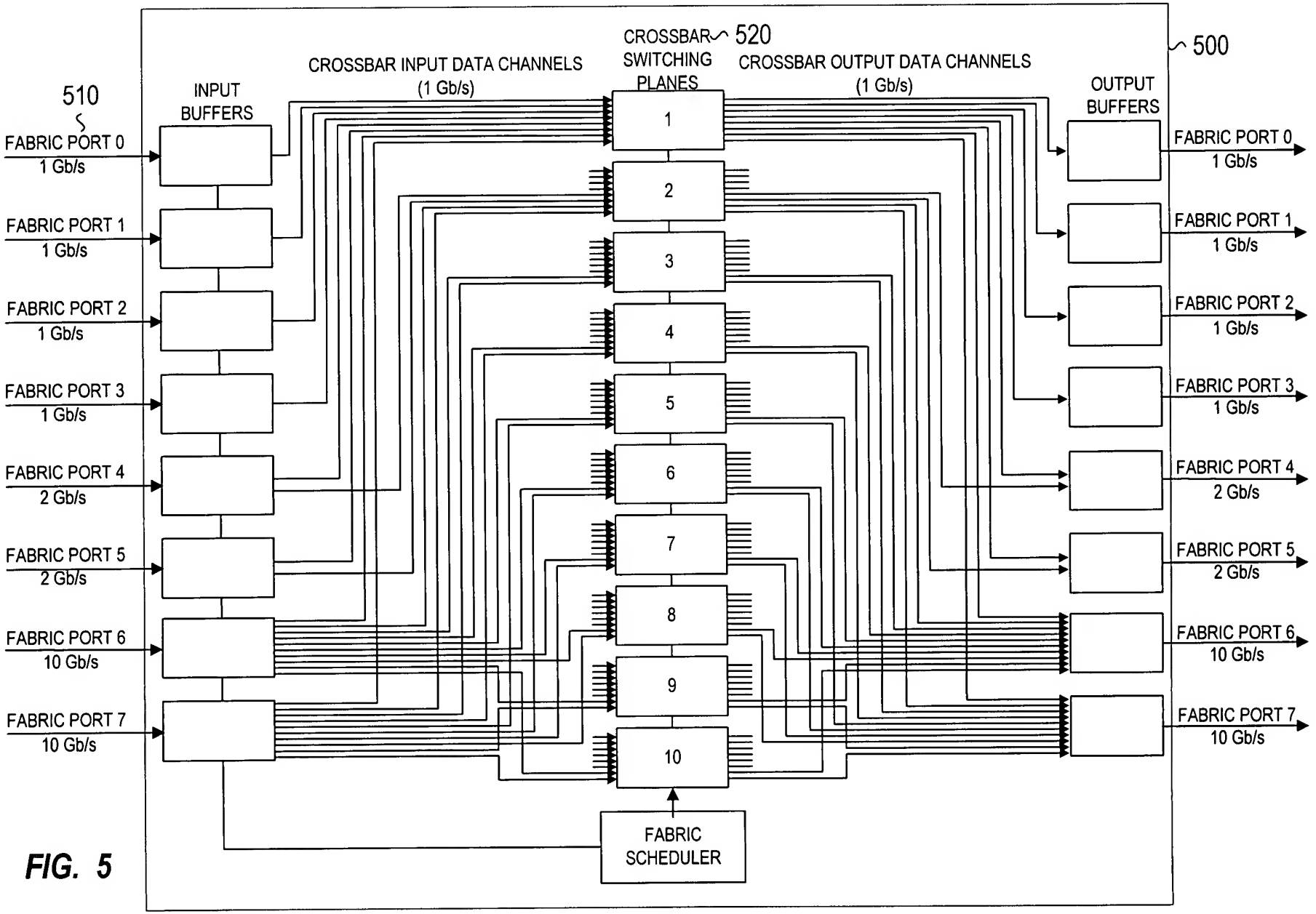

510
500
520
CROSSBAR SWITCHING PLANES
CROSSBAR INPUT DATA CHANNELS (1 Gb/s)
CROSSBAR OUTPUT DATA CHANNELS (1 Gb/s)
INPUT BUFFERS
OUTPUT BUFFERS
FABRIC PORT 0 1 Gb/s
FABRIC PORT 1 1 Gb/s
FABRIC PORT 2 1 Gb/s
FABRIC PORT 3 1 Gb/s
FABRIC PORT 4 2 Gb/s
FABRIC PORT 5 2 Gb/s
FABRIC PORT 6 10 Gb/s
FABRIC PORT 7 10 Gb/s
1
2
3
4
5
6
7
8
9
10
FABRIC SCHEDULER
FABRIC PORT 0 1 Gb/s
FABRIC PORT 1 1 Gb/s
FABRIC PORT 2 1 Gb/s
FABRIC PORT 3 1 Gb/s
FABRIC PORT 4 2 Gb/s
FABRIC PORT 5 2 Gb/s
FABRIC PORT 6 10 Gb/s
FABRIC PORT 7 10 Gb/s

FIG. 5

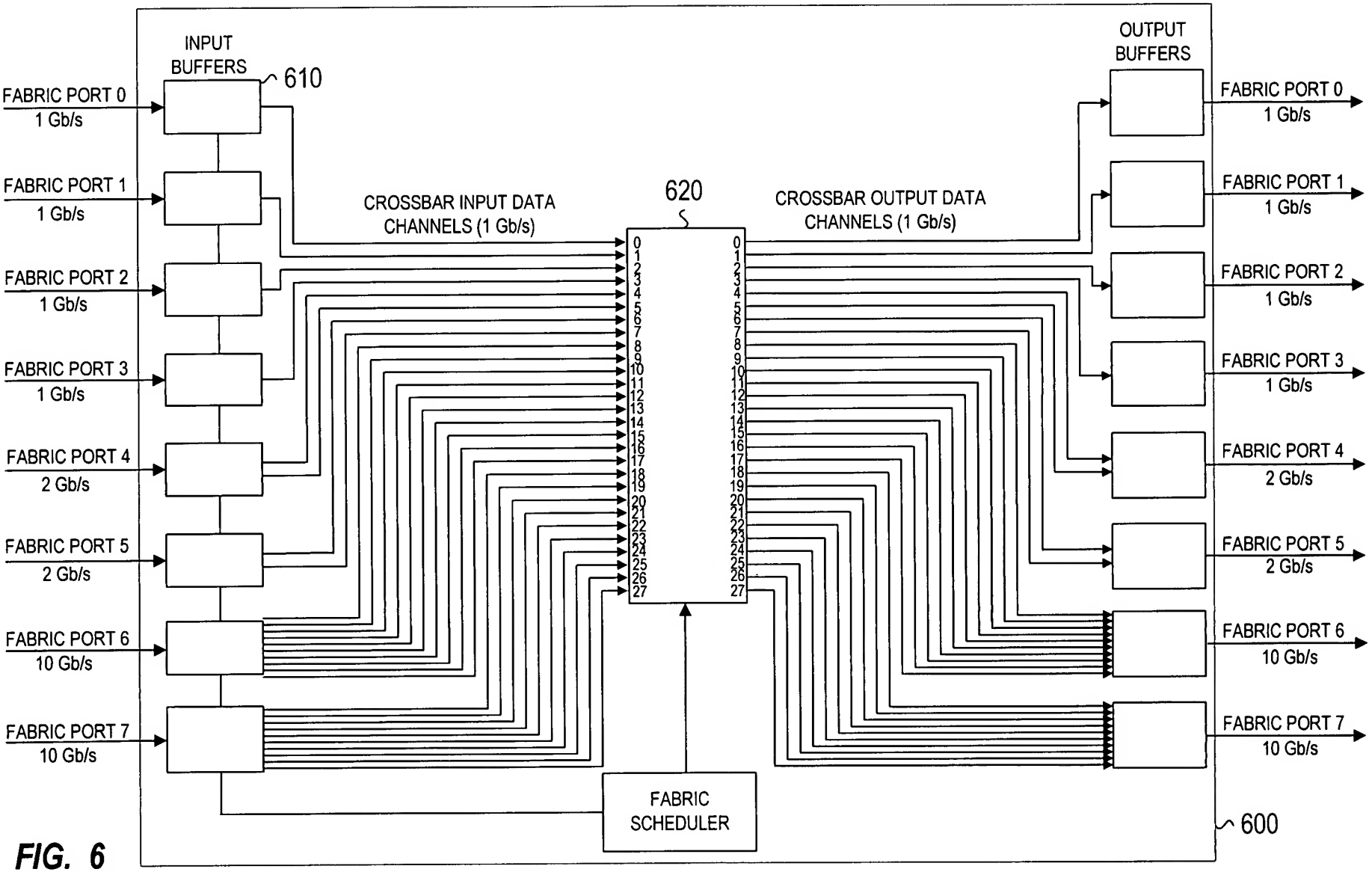

INPUT BUFFERS
610
OUTPUT BUFFERS
FABRIC PORT 0
1 Gb/s
FABRIC PORT 1
1 Gb/s
FABRIC PORT 2
1 Gb/s
FABRIC PORT 3
1 Gb/s
FABRIC PORT 4
2 Gb/s
FABRIC PORT 5
2 Gb/s
FABRIC PORT 6
10 Gb/s
FABRIC PORT 7
10 Gb/s
CROSSBAR INPUT DATA CHANNELS (1 Gb/s)
620
CROSSBAR OUTPUT DATA CHANNELS (1 Gb/s)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
FABRIC SCHEDULER
600

FIG. 6

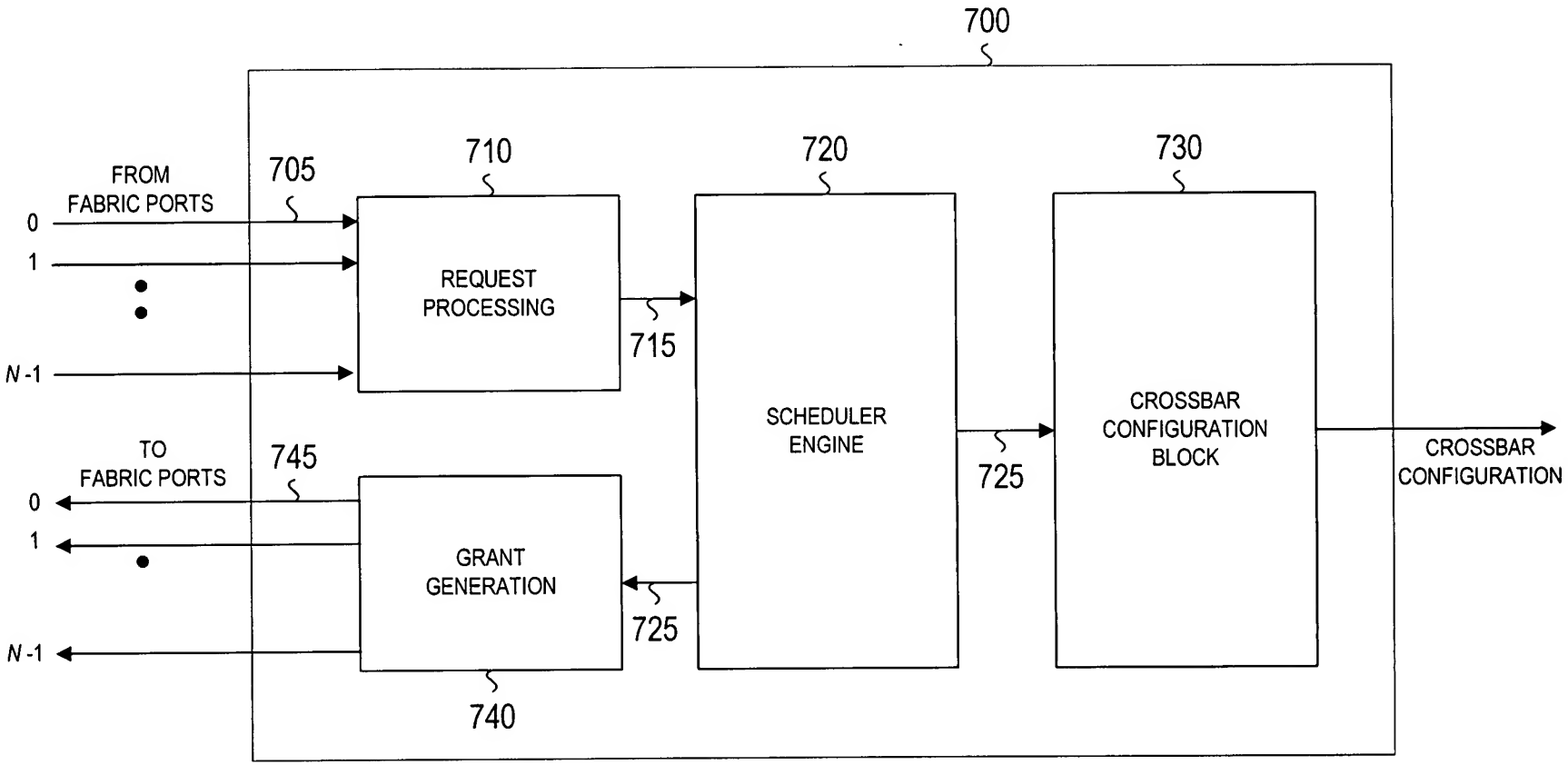
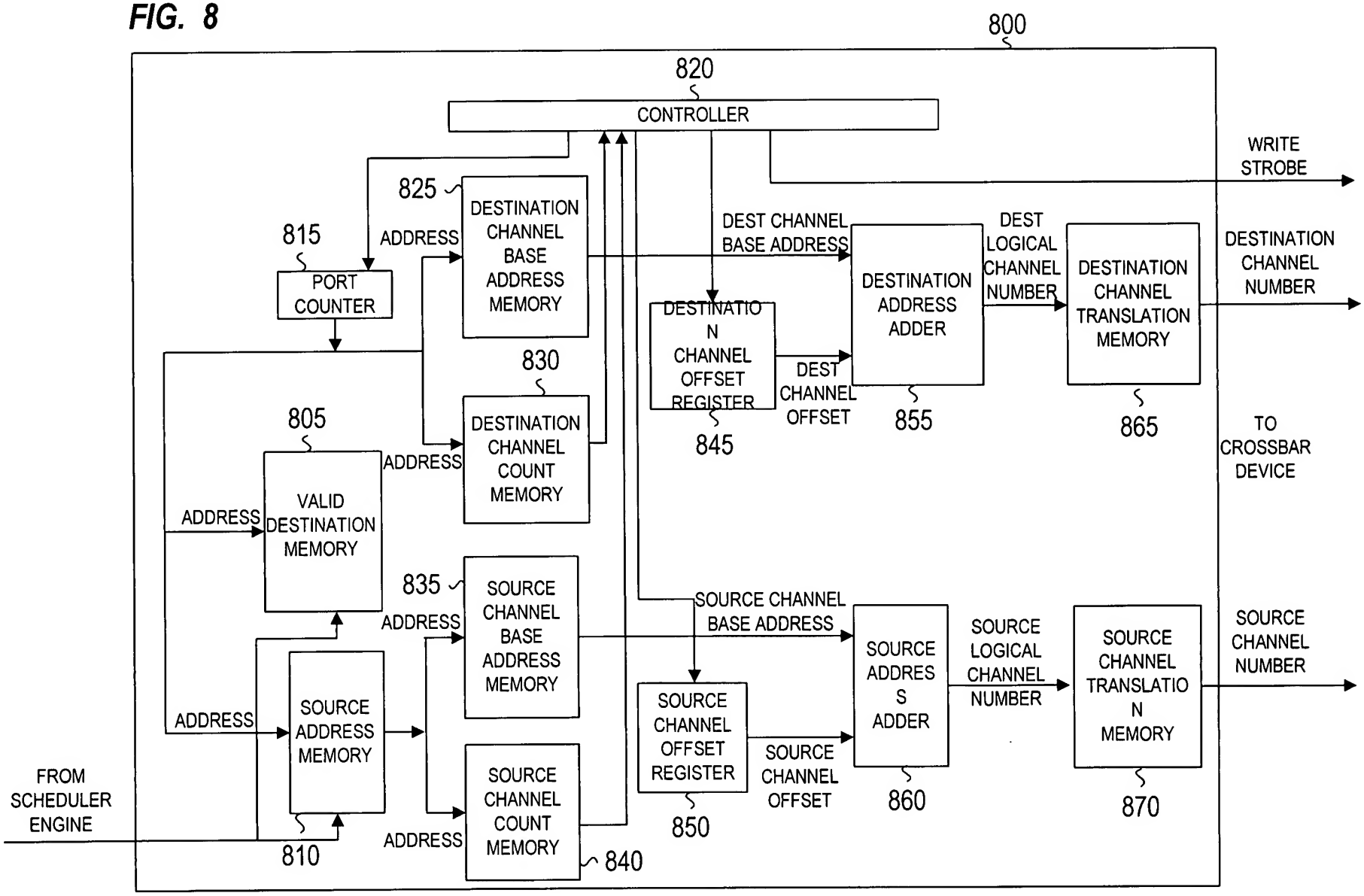

700
705
710
720
730
FROM
FABRIC PORTS
0
1
N-1
REQUEST
PROCESSING
715
SCHEDULER
ENGINE
725
CROSSBAR
CONFIGURATION
BLOCK
CROSSBAR
CONFIGURATION
745
TO
FABRIC PORTS
0
1
N-1
GRANT
GENERATION
725
740

FIG. 7

FIG. 8


800
820
CONTROLLER
WRITE STROBE
825
DESTINATION CHANNEL BASE ADDRESS MEMORY
ADDRESS
815
PORT COUNTER
DEST CHANNEL BASE ADDRESS
DESTINATION ADDRESS ADDER
DEST LOGICAL CHANNEL NUMBER
DESTINATION CHANNEL TRANSLATION MEMORY
DESTINATION CHANNEL NUMBER
DESTINATION CHANNEL OFFSET REGISTER
DEST CHANNEL OFFSET
855
865
845
830
805
DESTINATION CHANNEL COUNT MEMORY
ADDRESS
TO CROSSBAR DEVICE
VALID DESTINATION MEMORY
ADDRESS
835
SOURCE CHANNEL BASE ADDRESS MEMORY
ADDRESS
SOURCE CHANNEL BASE ADDRESS
SOURCE ADDRESS ADDER
SOURCE LOGICAL CHANNEL NUMBER
SOURCE CHANNEL TRANSLATION MEMORY
SOURCE CHANNEL NUMBER
SOURCE ADDRESS MEMORY
ADDRESS
SOURCE CHANNEL OFFSET REGISTER
SOURCE CHANNEL OFFSET
860
870
850
FROM SCHEDULER ENGINE
SOURCE CHANNEL COUNT MEMORY
ADDRESS
810
840

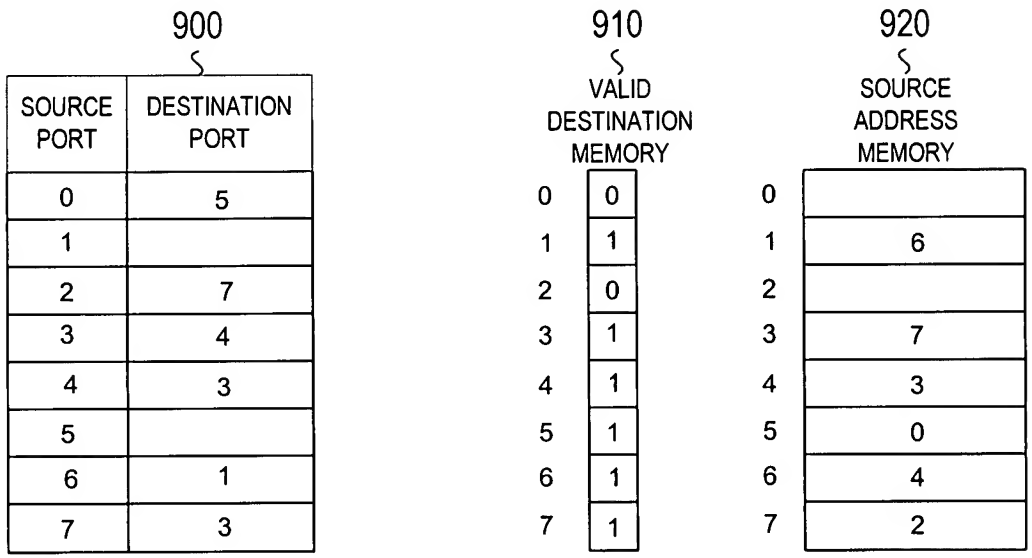

900
SOURCE PORT
DESTINATION PORT
0 5
1
2 7
3 4
4 3
5
6 1
7 3
910
VALID DESTINATION MEMORY
0 0
1 1
2 0
3 1
4 1
5 1
6 1
7 1
920
SOURCE ADDRESS MEMORY
0
1 6
2
3 7
4 3
5 0
6 4
7 2

FIG. 9

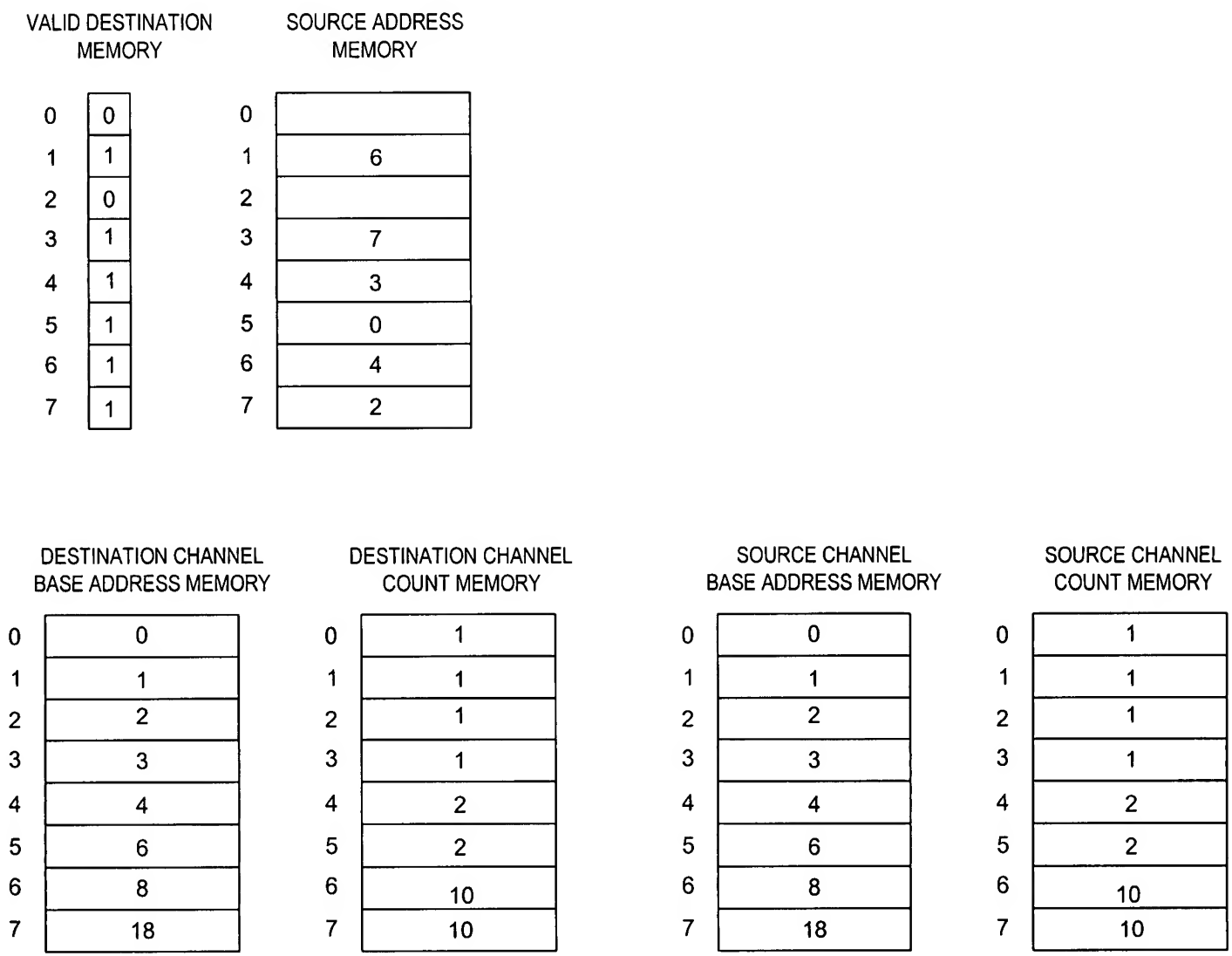

VALID DESTINATION MEMORY
SOURCE ADDRESS MEMORY
0 0
1 1
2 0
3 1
4 1
5 1
6 1
7 1
0
1 6
2
3 7
4 3
5 0
6 4
7 2
DESTINATION CHANNEL BASE ADDRESS MEMORY
0 0
1 1
2 2
3 3
4 4
5 6
6 8
7 18
DESTINATION CHANNEL COUNT MEMORY
0 1
1 1
2 1
3 1
4 2
5 2
6 10
7 10
SOURCE CHANNEL BASE ADDRESS MEMORY
0 0
1 1
2 2
3 3
4 4
5 6
6 8
7 18
SOURCE CHANNEL COUNT MEMORY
0 1
1 1
2 1
3 1
4 2
5 2
6 10
7 10

FIG. 10

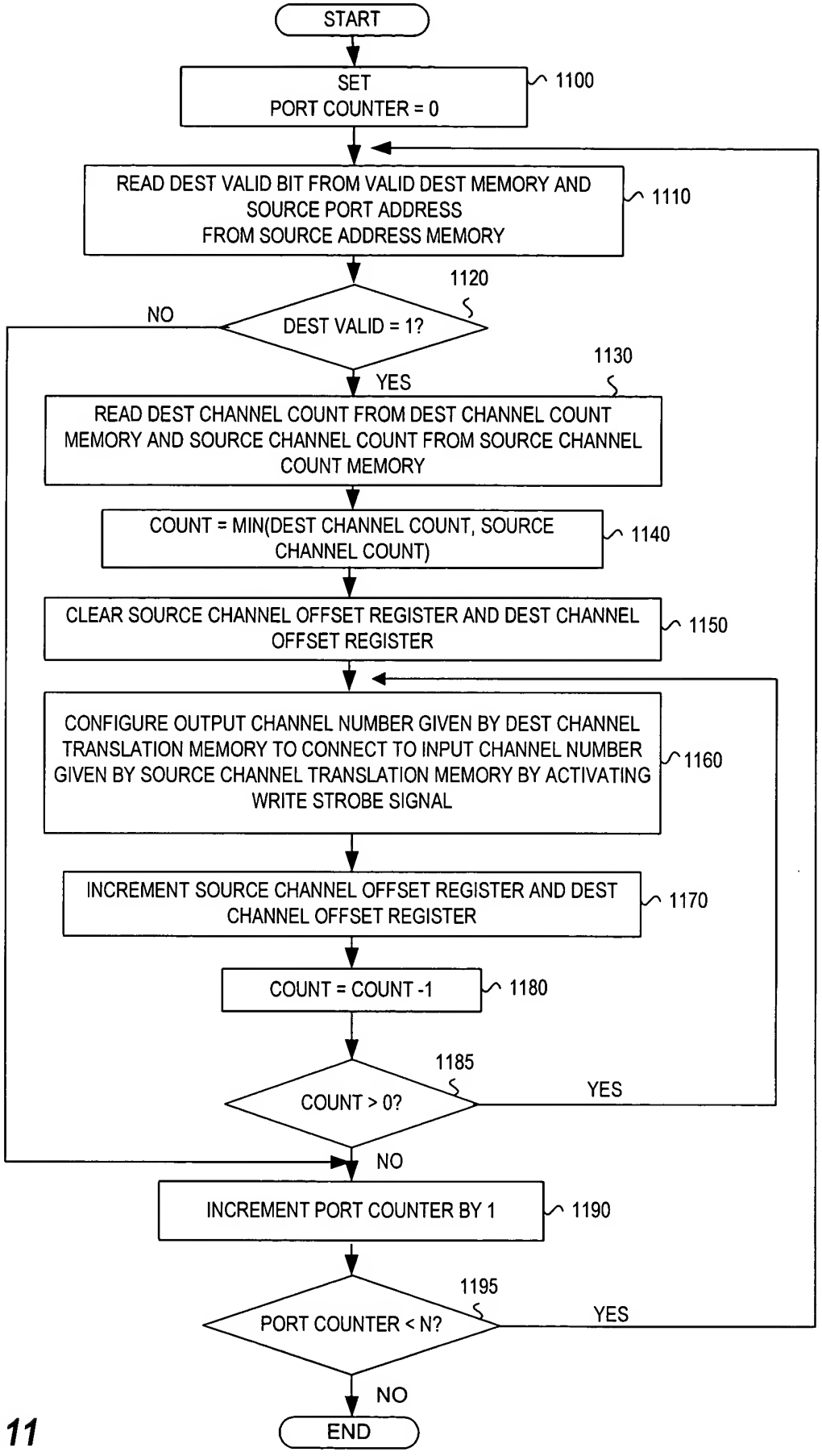

START
SET
PORT COUNTER = 0
1100
READ DEST VALID BIT FROM VALID DEST MEMORY AND
SOURCE PORT ADDRESS
FROM SOURCE ADDRESS MEMORY
1110
1120
DEST VALID = 1?
NO
YES
1130
READ DEST CHANNEL COUNT FROM DEST CHANNEL COUNT
MEMORY AND SOURCE CHANNEL COUNT FROM SOURCE CHANNEL
COUNT MEMORY
COUNT = MIN(DEST CHANNEL COUNT, SOURCE
CHANNEL COUNT)
1140
CLEAR SOURCE CHANNEL OFFSET REGISTER AND DEST CHANNEL
OFFSET REGISTER
1150
CONFIGURE OUTPUT CHANNEL NUMBER GIVEN BY DEST CHANNEL
TRANSLATION MEMORY TO CONNECT TO INPUT CHANNEL NUMBER
GIVEN BY SOURCE CHANNEL TRANSLATION MEMORY BY ACTIVATING
WRITE STROBE SIGNAL
1160
INCREMENT SOURCE CHANNEL OFFSET REGISTER AND DEST
CHANNEL OFFSET REGISTER
1170
COUNT = COUNT -1
1180
1185
COUNT > 0?
YES
NO
INCREMENT PORT COUNTER BY 1
1190
1195
PORT COUNTER < N?
YES
NO
END

FIG. 11